REMARKS

Claims 9-11 are pending in the application. By this amendment, claim 9 is being amended to improve its form; a marked up version of the amended claim is attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). No new matter is involved.

On page 2 of the Office Action, the drawings which include color photographs are objected to. Such objection has been duly noted Applicants. Upon allowance of the application, Applicants will file a Petition under 37 C.F.R. § 1.84(a)(2).

The priority acknowledgment at the top of page 3 of the Office Action has been noted.

At the bottom of page 3 of the Office Action, claim 9 is rejected under 35 U.S.C. § 102(a) as being anticipated by Kamiya et al. At the top of page 4 of the Office Action, claims 9-11 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,432,122 of Chae. Such rejections are respectfully traversed.

Transistor devices in accordance with the invention are configured with a top-gate structure comprising a gate electrode formed over the polycrystal semiconductor layer with a gate insulation film disposed therebetween. In the cited art, on the other hand, the transistor is configured with a bottom-gate structure.

This is particularly true of Chae. In a bottom-gate structure in which the gate electrode is positioned below the a-Si film, heat generated by laser irradiation dissipates more quickly in the region of the a-Si film directly above the gate electrode than in other regions of the a-Si film. This is because of heat conduction via the gate electrode. Consequently, grain size differences are created between the

p-Si film formed directly above the gate electrode and the p-Si film formed on both sides of the gate electrode, which in turn results in the disadvantage of unevenness in the TFT characteristics within the plane. In contrast, when a top-gate structure is employed, the laser is irradiated on the a-Si film formed below the gate electrode. According to this configuration, laser annealing can be performed without a metal material having high heat conductivity located locally beneath the a-Si film. The disadvantages of the bottom-gate structure as described above can therefore be avoided.

Claim 9 is being amended in order more clearly distinguish patentably over the art. More particularly, claim 9 is being amended to clarify that the transistor device is configured with a top-gate structure comprising a gate electrode formed over the polycrystal semiconductor layer with a gate insulation film disposed therebetween. As amended claim 9 contains the further limitation "and a gate electrode is formed over the active layer with a gate insulation film disposed therebetween". This further defines the transistor device (the product of claim 9 and not the method of making it) in terms of the top-gate structure in accordance with the invention. As so amended, claim 9 is submitted to clearly distinguish patentably over the art, for the reasons set forth above. Claims 10 and 11 each depend from claim 9 and contain all of the limitations thereof. Consequently, claims 10 and 11 are also submitted to clearly distinguish patentably over the art.

In conclusion, claims 9-11 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Date: December 20, 2002

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Version with markings to show changes made:

Rewrite claim 9 as follows:

9. (Amended) A transistor device in which a polycrystal semiconductor layer is formed by subjecting an amorphous semiconductor layer formed on a substrate to laser anneal processing, wherein

an energy level in a region to be irradiated by a laser beam of the amorphous semiconductor layer is set such that the level in a rear area of a region along a scan direction of the laser beam is lower than the upper limit energy level which maximizes a grain size of the semiconductor layer, and

the amorphous semiconductor layer is annealed by the laser beam and the polycrystal semiconductor layer obtained is used as an active layer of the transistor device, and a gate electrode is formed over the active layer with a gate insulation film disposed therebetween.